Paper No. 38

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YUKIO MAKI

Appeal No. 2001-1523
Application No. 08/731,236

HEARD: May 8, 2002

Before HAIRSTON, LALL, and BARRY, Administrative Patent Judges

LALL, Administrative Patent Judge.

DECISION ON APPEAL[1]

This is a decision on appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1 through 16 and 18 through 24, all the pending claims in the application.

[1]Appellant points out on page 1 of the reply brief that the examiner has not acknowledged the IDS of August 13, 1998. We will leave this issue to the examiner, it being a procedural issue. Therefore, any applicable art contained therein is not before us in this appeal.

The disclosed invention is directed to a manufacturing process for a semiconductor device having semiconductor memories and bipolar transistors. The process includes forming contact holes for the semiconductor memories in an insulating film, and concurrently forming a plurality of openings in an insulating film, and forming bipolar transistors at the locations of the additional openings. In specific embodiments, appellant's claimed method includes forming the bipolar transistors with characteristics different from each other.

Further understanding of the invention can be obtained by reading the following claim.

> 1. A manufacturing process for a semiconductor device having a semiconductor memory circuit region containing semiconductor memories, and a peripheral circuit region disposed around said semiconductor circuit region and containing bipolar transistors, said process comprising the steps of:
>
> forming contact holes, for said semiconductor memories, selectively in an insulating film in said semiconductor memory circuit region;
>
> forming a plurality of openings selectively in an insulating film, concurrently with forming one of said contact holes, in bipolar transistor forming regions;
>
> forming contact conductors in said contact holes; and

forming bipolar transistors at the locations of said openings in said bipolar transistor forming regions by implanting impurities through at least one of said plurality of openings.

The examiner relies on the following references:

Komatsu	4,589,936	May 20, 1986
Christenson	4,882,294	Nov. 21, 1989
Shiomi et al. (Shiomi)	5,095,355	Mar. 10, 1992

Claims 1 and 12 rejected under 35 U.S.C. § 103 as being unpatentable over Shiomi. Claims 1 and 12 also stand rejected under 35 U.S.C. § 103 as being unpatentable over Christenson[2].

Claims 1 through 16, and 18 through 24 stand rejected under 35 U.S.C. § 103 as being unpatentable over Christenson in view of Komatsu.

Rather than repeat the arguments of appellants and the examiner, we make reference to the briefs[3] and the answer for the respective details thereof.

[2] The examiner has not reproduced this rejection in the examiner's answer, however, the examiner responds to the arguments by appellant regarding this rejection at pages 7 and 8 of the examiner's answer. Therefore, we assume that the examiner is still maintaining this rejection as presented in the final rejection and as responded to by appellant.

[3] A reply brief was filed as paper no. 32 on May 25, 2001. The examiner noted the entry of the reply brief, see paper no. 33.

OPINION

We have considered the rejections advanced by the examiner and the supporting arguments. We have, likewise, reviewed the appellant's arguments set forth in the briefs.

We reverse.

In our analysis, we are guided by the general proposition that in an appeal involving a rejection under 35 U.S.C. § 103, an examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). We are further guided by the precedent of our reviewing court that the limitations from the disclosure are not

to be imported into the claims. In re Lundberg, 244 F.2d 543, 113 USPQ 530 (CCPA 1957); In re Queener, 796 F.2d 461, 230 USPQ 438 (Fed. Cir. 1986). We also note that the arguments not made separately for any individual claim or claims are considered waived. See 37 CFR § 1.192(a) and (c). In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobviousness distinctions over the prior art."); In re Wiechert, 370 F.2d 927, 936, 152 USPQ 247, 254 (CCPA 1967)("This court has uniformly followed the sound rule that an issue raised below which is not argued in that court, even if it has been properly brought here by reason of appeal is regarded as abandoned and will not be considered. It is our function as a court to decide disputed issues, not to create them.").

Consistent with the categorization of the three rejections in the case by both appellant and the examiner, we consider the different rejections below.

Shiomi

The examiner rejects claims 1 and 12 under this reference at pages 3 and 4 of the examiner's answer. The examiner asserts (id. at page 4) that "Shiomi lacks anticipation for implanting selectively prior to the formation of the insulating film . . . . . However, the selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results." Appellant argues (brief at page 6) that "[o]n the contrary, in Shiomi et al's method, transistors are formed before forming the metal contacts. Furthermore, Shiomi et al's bipolar transistors are formed using a plurality of implanting steps through different holes formed in different resists. Therefore, in Shiomi et al's method, bipolar transistors are not formed at the locations of openings having been concurrently formed with forming contact holes for semiconductor memories." Appellant further argues (brief at page 7) that "absent improper hindsight, there is no evidence of clear suggestion either in the Shiomi et al patent or within the record to perform the steps recited in Applicant's Claims 1 and

12 . . . . Applicant's invention is therefore not achievable by merely re-ordering Shiomi et al's steps, and such re-ordering is not suggested . . . ." The examiner responds (answer at page 6) that "[i]n the instant case, Shiomi et al. clearly discloses, forming a plurality of openings selectively in an insulating film . . ., concurrently forming one of said contact holes, in bipolar transistors forming region . . ., as cited in claim 1." Appellant responds (reply brief at page 3) that "Shiomi et al fail to teach or suggest forming bipolar transistors at locations of openings formed concurrently with forming contact holes, ..."

We have reviewed the Shiomi patent, especially columns 7 and 8 where the process of Figs. 5A through 5G is explained. We do not find that the forming of the contact conductors in the contact holes and the forming of bipolar transistors are concurrently performed in Shiomi's process. In Shiomi, the metallization of the contact holes is performed after all the transistors have been made. The examiner's assertion that the recited process is a mere re-ordering of the steps in a complex

process such as the efficient manufacturing of the memory components is sheer speculation. Therefore, we do not sustain the obviousness rejection of claims 1 and 12 over Shiomi.

Christenson

The examiner rejects claims 1 and 12 under this reference at page 3 of the final rejection (paper no. 24). Appellant argues in response (brief at page 9) that "[f]irst, Christenson is silent on forming semiconductor memories. Therefore, contrary to the outstanding Office Action's statement at page 3, Christenson fails to teach forming contact holes in a semiconductor memory circuit region, as recited in Applicant's claims. . . . Second, Christenson does not form bipolar transistors at the locations of openings formed concurrently with contact holes for semiconductor memories. Christenson forms individual regions . . . ." The examiner responds first that since Christenson teaches the making of an integrated circuit involving capacitors, resistances, and transistors, it would have been obvious to an artisan to utilize Christenson's teachings in making a memory involving a memory region; secondly, that

Christenson does teach the steps of making bipolar transistors, see answer at pages 7 and 8.

We are not persuaded by the examiner's position. We, instead, agree with appellant that Christenson merely teaches the forming of a semiconductor integral circuit device and does not even describe the concept of a semiconductor memory, let alone the specific recited process. Furthermore, we also agree with appellant that Christenson does not suggest concurrent making of the contact hole metallization with the making of the bipolar transistors. Therefore, we do not sustain the rejection of claims 1 and 12 over Christenson.

Christenson and Komatsu

The examiner rejects claims 1 through 16 and 18 through 24 over this combination at pages 4 and 5 of the examiner's answer. After considering the appellant's arguments (brief at page 10) and the examiner's response (answer at page 9), we conclude that the rejection is not sustainable because Komatsu does not cure the deficiency of Christenson as noted above.

The decision of the examiner rejecting claims 1 through 16 and 18 through 24 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
PARSHOTAM S. LALL Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

vsh

OBLON, SPIVAK, MCCLELLAND,
MAIER & NEUSTADT
1755 JEFFERSON DAVIS HIGHWAY
FOURTH FLOOR
ARLINGTON, VA 22202